9997 FOUR BIT SHIFT REGISTER

INDUSTRIAL MICROLOGIC® INTEGRATED CIRCUIT

OPERATING TEMPERATURE RANGE 0°C TO 70°C

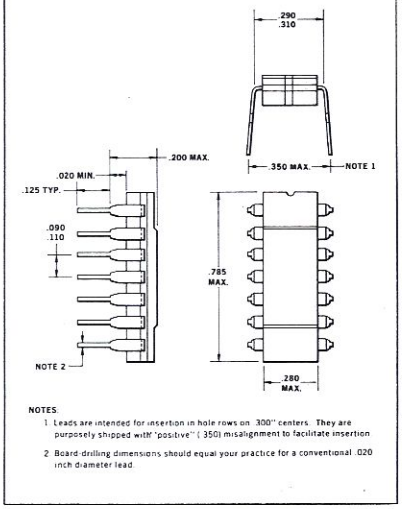
GENERAL DESCRIPTION — The Micrologic® Integrated Circuit Four-Bit Shift Register is a fully integrated, monolithic digital circuit which is manufactured using the patented Fairchild Planar* epitaxial process.

THE 9997 FOUR-BIT SHIFT REGISTER consists of four series connected Flip-Flops and the circuitry required for triggering and resetting the Flip-Flops. Each Flip-Flop has a common reset input, a parallel (asynchronous) input, data input, and a non-inverted, buffered output which receives power from a separate voltage supply (V_{CC}') that is common to all outputs.

The separate voltage supply (V_{CC}') is independent of the V_{CC} terminal, i.e., the circuit will operate with $V_{CC} = 5.5V$ and $V_{CC}' = 3.3V$ or $V_{CC} = 3.3V$ and $V_{CC}' = 5.5V$, etc.

Typical applications include: Serial shifting, parallel shifting (static storage register), serial input-parallel output, parallel input-serial output, and shift counters.

TYPICAL DUAL IN-LINE PACKAGE
(In accordance with JEDEC TO–116)



NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.350) misalignment to facilitate insertion.
2. Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

PURCHASING INFORMATION:
To order this device specify U6A999729X.

FEATURES

- **SERIAL OPERATION WITH PARALLEL ENTRY TO ALL BITS**
- **ASYNCHRONOUS GANGED RESET CAPABILITY**
- **WIDE V_{CC} RANGE — COMPATIBLE OPERATION WITH SEVERAL LOGIC FAMILIES**
- **OUTPUTS CAN BE GATED**
- **SINGLE LINE SERIAL INPUT**
- **HANDLES BLOCKS OF FOUR BITS OF DATA COMMON TO MANY PARALLEL/SERIAL AND SERIAL/PARALLEL OPERATIONS**
- **CAN DRIVE 40 CCSL UNIT LOADS**

ELECTRICAL CHARACTERISTICS

Operating Voltage Range	3.3 to 5.5 Volts
Minimum Shifting Rate	D.C. to 5.0 MHz
Typical Shifting Rate	D.C. to 7.0 MHz
Maximum Power Dissipation ($V_{CC}' = V_{CC}$)	380 mW
Maximum Power Dissipation ($V_{CC}' =$ open)	260 mW

NORMAL OPERATION

SERIAL SHIFTING — A high to low voltage transition at the trigger input (T) initiates the following simultaneous state transfers: $D \rightarrow Q_1$, $Q_1 \rightarrow Q_2$, $Q_2 \rightarrow Q_3$, and $Q_3 \rightarrow Q_4$.

RESET AND PARALLEL ENTRY — A high voltage level at the reset input (R) overrides all other inputs and causes all four Flip-Flops to be reset such that the Q_1, Q_2, Q_3, and Q_4 outputs assume a high voltage level and remain high after removal of the reset signal. After removal of the reset signal, a high voltage level at a set input (S_1 through S_4) will cause each Flip-Flop to be set such that its corresponding output (Q_1 through Q_4) will be at a low voltage level. No change of state will occur if a set input is at a low signal level.

Note that since the buffered outputs receive power from a separate voltage supply they can be gated (or enabled) by gating the voltage applied to Pin 13. This feature is useful from a logical viewpoint, as well as a power conservation consideration. The gated emitter-follower circuit shown on the back of this sheet is recommended.

* Planar is a patented Fairchild process.

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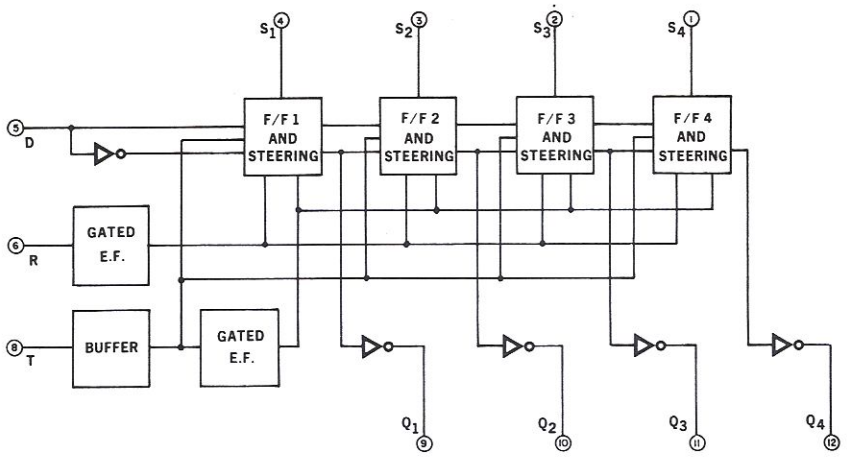
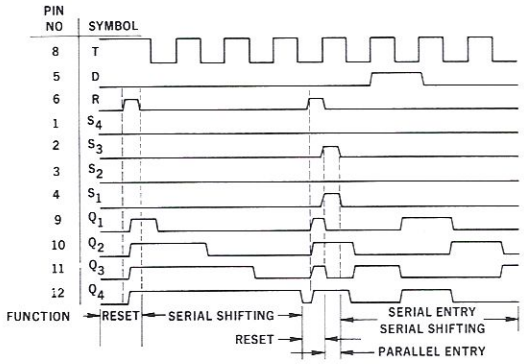
BLOCK DIAGRAM

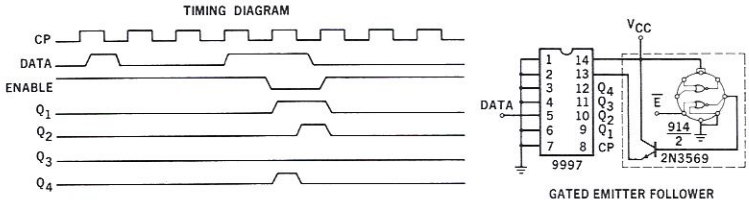


FOUR BIT SHIFT REGISTER (PRODUCT CODE 9997) BLOCK DIAGRAM

TYPICAL TIMING DIAGRAM

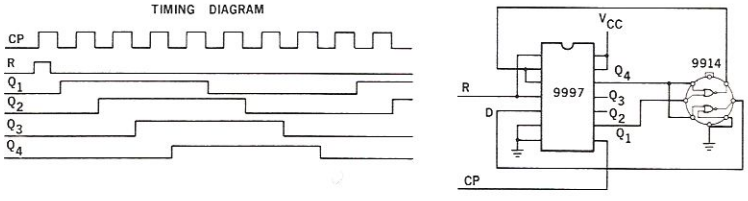


SERIAL SHIFT REGISTER WITH GATED OUTPUTS.



GATED EMITTER FOLLOWER

MODULO 8 SHIFT REGISTER COUNTER
(Shifting Rate Test Circuit)



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